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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,031	03/31/2004	Hiroki Goko	030712-36	3838

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EXAMINER	
MEMULA, SURESH	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,031	GOKO ET AL.	
	Examiner	Art Unit	
	Suresh Memula	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Paul Dinh
Primary Examiner

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/31/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: On page 29, line 14 "cock" is a spelling error and should be changed to "clock". On page 2, line 3 "descried" is a spelling error and should be changed to "described".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In Claim 1, "the number of clocks" on line 3, "the timings" on line 11, "the constraints" on line 15, and "the constraint violation" on line 17 are limitations that lack antecedent basis.

In Claim 2, "said different clocks" on line 25, and "the respective timings" on line 8 are limitations that lack antecedent basis.

In Claim 3, the limitation "the value...the clock delays" on lines 14-15 lacks antecedent basis.

In Claim 4, the limitation "said clocks" on line 21 lacks antecedent basis.

In Claim 5, "the output" on line 25, and "the allocated clock delays" on line 2 are limitations that lack antecedent basis.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Li et al. (US Patent. No. 5,974,245).

As to Claim 1,

a first step for determining the number of clocks different in delay amount (FIG. 3), which are used for verification of a circuit design of the semiconductor integrated

circuit upon the circuit design thereof (Abstract, and FIG. 4-5 and 7) and determining delays in the clocks on the basis of pre-set conditions for constraints of timings (Abstract, Col. 1 lines 14-21 and 28-36, and FIG. 1, 4-5, 7, and 9);

a second step for allocating clocks supplied to respective circuits (Col.1 lines 50-53, FIG. 3, and 9-11); and

a third step for optimizing the timings on the basis of a list obtained by the timing constraint conditions and the clock allocation (Abstract, and FIG. 4, and 7-11) and determining whether results of analyses of the respective timings correspond to violation of the constraints (FIG. 4-5, and 7-11), wherein the optimization of the timings is repeated according to the constraint violation (Claim 20, and FIG. 4-5, 7, and 9-11).

As to Claim 2,

a fourth step for generating the clocks different in the delay amount for the verification of a layout design of the semiconductor integrated circuit upon the layout design thereof (Col. 4 lines 42-47, and FIG. 1, and 4);

a fifth step for adjusting skews every said different clocks (Abstract, Col. 2 lines 50-53, Col. 3 lines 6-10, Claim 8 and 13, and FIG. 5 and 7);

a sixth step for adjusting delays respectively included in the clocks to the determined clock delays upon the layout design, respectively (Abstract, Col. 3 lines 6-10, Claims 8 and 13, and FIG. 5);

seventh step for making an adjustment to a layout that satisfies the timing constraint conditions upon the layout design and determining whether analytical results of the respective timings correspond to the constraint violation (Col. 6 lines 27-34 and

47-55, and FIG. 4), wherein the layout adjustment is repeated according to the constraint violation (Col. 6 lines 47-55, and FIG. 7 and 9-11).

As to Claim 3, adjusting the value of each of the clock delays again according to the constraint violation when the constraint violation exists in the third step (Col. 6 lines 35-45, and FIG. 3-4, and 7-10).

As to Claim 4, a method according to claim 1, further comprising a ninth step for adjusting delays set every said clocks according to the constraint violation when the constraint violation occurs in the seventh step (FIG. 4-6).

As to Claim 5, a method according to claim 1, which adds a delay taken up to the output of data at a starting point where the data is outputted, a time interval required to set up the data, a delay developed with a path between respective circuits and a delay in the clock to be used, and determines the allocated clock delays according to the difference between the added value and the cycle of the clock (Col 3. 6-10, and Col. 4 lines 30-34).

Claims 1, 3, and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Tetelbaum (US Pub. No. 2005/0050497).

As to Claim 1,

a first step for determining the number of clocks different in delay amount (See one or more of paragraphs 0049, 0055-0057, 0075, 0077, and FIG. 3,5, and 8-10), which are used for verification of a circuit design of the semiconductor integrated circuit upon the circuit design thereof (FIG. 1 and 11) and determining delays in the clocks on the basis of pre-set conditions for constraints of timings (FIG. 11);

a second step for allocating clocks supplied to respective circuits (Paragraph 0002, and FIG. 3, 5, 7-11, 13, and 16-17); and

a third step for optimizing the timings on the basis of a list obtained by the timing constraint conditions and the clock allocation (FIG. 11) and determining whether results of analyses of the respective timings correspond to violation of the constraints (FIG. 11), wherein the optimization of the timings is repeated according to the constraint violation (FIG. 11).

As to Claim 3, adjusting the value of each of the clock delays again according to the constraint violation when the constraint violation exists in the third step (FIG. 11)

As to Claim 5, a method according to claim 1, which adds a delay taken up to the output of data at a starting point where the data is outputted, a time interval required to set up the data, a delay developed with a path between respective circuits and a delay in the clock to be used, and determines the allocated clock delays according to the difference between the added value and the cycle of the clock (Paragraphs 0069,0106, 0012, 0114, and FIG. 9-13).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh Memula whose telephone number is (571) 272-8046. The examiner can normally be reached on M-F 8am-4:30pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SM
02/14/2006

Paul Dinh

Primary Examiner